CSE 206 (Digital Logic Design Sessional)

Experiment No.: 02

Name of the Experiment:

**Truth tables and simplification using Boolean Algebra**

|  |  |
| --- | --- |
| Group No.: | 06 |
| Writers’ Roll: | 1805116  1805120 |
| Section: | B2 |
| Department: | CSE |
| Other Group Members: | 1805117  1805118  1805119  1705107 |
| Date of Performance: | 10/03/2021 |
| Date of Submission: | 13/03/2021 |

**Problem No.1:**

**Problem Specification:**

Simplify the equation using Boolean algebra and implement it.

F (A, B, C, D) = A’B’C’D’ + ABCD + ABC’D + A’B’CD’ + A’BC’D + AB’C’D’ + AB’CD’ + A’BCD

**Required Instruments:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No** | **Name** | **Model** | **Quantity** |
| 01 | Logisim Software |  |  |
| 02 | IC(Hex-Inverter) | 74LS04 | 01 |
| 03 | IC (Quad 2 input AND) | 74LS08 | 01 |
| 04 | IC (Quad 2 input OR) | 74LS32 | 01 |
| 05 | Wires |  |  |
| 06 | Input Pins |  | 04 |
| 07 | Output Pins |  | 01 |

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F (A, B, C, D)** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Required Equation:**

F (A, B, C, D) = A’B’C’D’ + ABCD + ABC’D + A’B’CD’ + A’BC’D + AB’C’D’ + AB’CD’ +

A’BCD

= A’B’C’D’+A’B’CD’+ABCD+ABC’D+A’BC’D+A’BCD+AB’C’D’+AB’CD’  
 = A’B’D’(C’+C)+ABD(C+C’)+A’BD(C’+C)+AB’D’(C’+C)

= A’B’D’+ABD+A’BD’+AB’D’

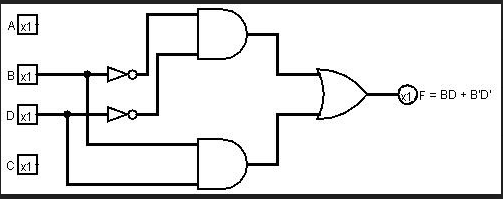
= A’B’D’+AB’D’+ABD+A’BD

= B’D’(A’+A)+BD(A+A’)

= B’D’+BD

= (B ⊕ D)’

**Circuit Diagram:**



**Observations:**

1. We tried to make the circuit in such a way that it was not too dense with wires
2. We used the documentations of the ICs to make sure the connections were given through the right pins
3. We checked the output according to the truth table

**Problem no.02**

**Problem specification:**

Derive the equations for a 3-bit gray to binary converter from Truth table and implement those with the required gates.

**Required Instruments:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No** | **Name** | **Model** | **Quantity** |
| 01 | Logisim Software |  |  |
| 02 | IC (Hex-Inverter) | 74LS04 | 01 |
| 03 | IC (Quad 2 input AND) | 74LS08 | 03 |
| 04 | IC (Quad 2 input OR) | 74LS32 | 01 |
| 05 | Wires |  |  |
| 06 | Input Pin |  | 03 |
| 07 | Output Pin |  | 03 |

**Truth table:**

Truth table for the 3-bit gray code to binary representation conversion is presented below. Here ABC is gray code and XYZ is its binary representation.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **X** | **Y** | **Z** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |

**Required Equation:**

**Equation for X:**

X = ABC’ + ABC + AB’C + AB’C’

= AB(C+C’) + AB’(C+C’)

= AB + AB’

= A(B+B’)

= A

**Equation for Y:**

Y = A’BC + A’BC’ + AB’C + AB’C’

= A’B (C + C’) + AB’ (C + C’)

= A’B + AB’

=A ⊕B

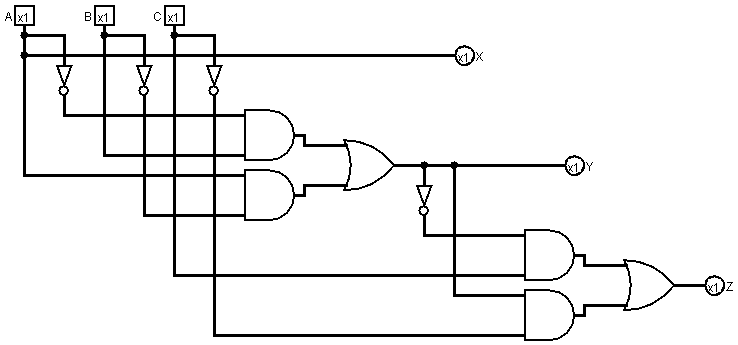
**Equation for Z:**

Z = A’B’C + A’BC’ + ABC + AB’C’

= A’ (B ⊕ C) + A (B ⊕ C)’

= A ⊕ (B ⊕ C)

**Circuit Diagram:**

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**Observation:**

1. We made a truth table and found out the output equations. We simplified the output equations and implemented the simplified form in our diagram.
2. We tried to make the circuit in such a way that it was not too dense with wires.
3. We used the documentations of the ICs to make sure the connections were given through the right pins.
4. We checked the output according to the truth table.

**Problem no.03**

**Problem specification:**

Derive the truth table and corresponding output equations for the given condition and implement those with the required gates.

Condition: There are 3 inputs into a system. The system will glow LED1 and LED0 in such a way that the pattern represents the number of set bits in the input.

**Required Instruments:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No** | **Name** | **Model** | **Quantity** |
| 01 | Logisim Software |  |  |
| 02 | IC (Hex-Inverter) | 74LS04 | 01 |
| 03 | IC (Quad 2 input AND) | 74LS08 | 02 |
| 04 | IC (Quad 2 input OR) | 74LS32 | 01 |
| 05 | Wires |  |  |
| 06 | Input Pin |  | 03 |
| 07 | Output Pin |  | 02 |

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **LED1** | **LED0** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Required Equation:**

**Equation for LED0:**

LED0 = A’B’C + A’BC’ + AB’C’ + ABC

= A’ (B ⊕ C) + A (B ⊕ C)’

= A ⊕ (B ⊕ C)

**Equation for LED1:**

LED1 = A’BC + AB’C + ABC’ + ABC

= BC (A + A’) + A (BC’ + B’C)

= BC + AB’C +ABC’

= C (B + AB’) + ABC’

= C (A+B) + ABC’

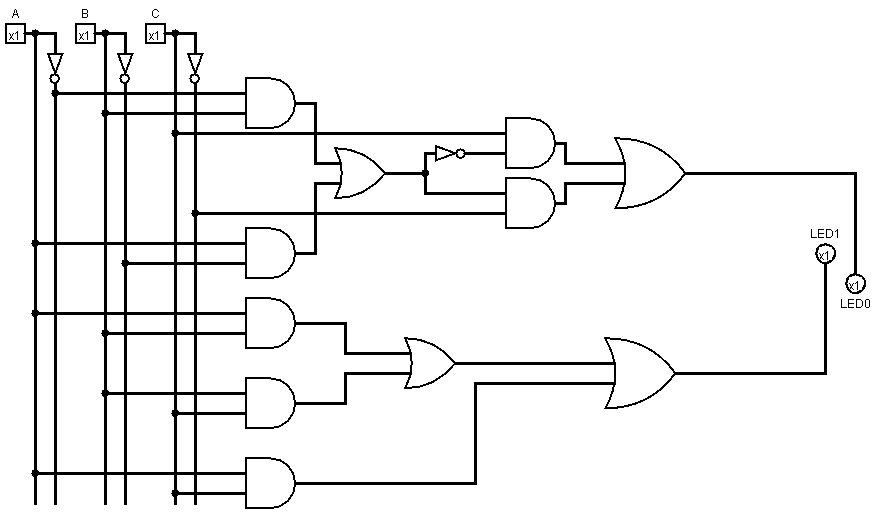
= AC + BC +ABC’

= BC + A (BC’ + C)

= BC + A(B+C)

= AB + BC + AC

**Circuit Diagram:**

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**Observation:**

1. We made a truth table and found out the output equations. We simplified the output equations and implemented the simplified form in our diagram.
2. We tried to make the circuit such a way that it was not too dense with wires
3. We used the documentations of the ICs to make sure the connections were given through the right pins.
4. We checked the output according to the truth table.

**Problem No.4:**

**Problem Specification:**

For the following logic function, find out the truth table, write down the logic expression. Simplify the logic expression as far as possible using Boolean algebra and then implement it.

F (A, B, C, D) =Σ (6, 9, 12, 15)

**Required Instruments:**

|  |  |  |  |
| --- | --- | --- | --- |
| **No** | **Name** | **Model** | **Quantity** |
| 01 | Logisim Software |  |  |
| 02 | IC(Hex-Inverter) | 74LS04 | 01 |
| 03 | IC (Quad 2 input AND) | 74LS08 | 02 |
| 04 | IC (Quad 2 input OR) | 74LS32 | 01 |
| 05 | Wires |  |  |
| 06 | Input Pins |  | 04 |
| 07 | Output Pins |  | 01 |

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

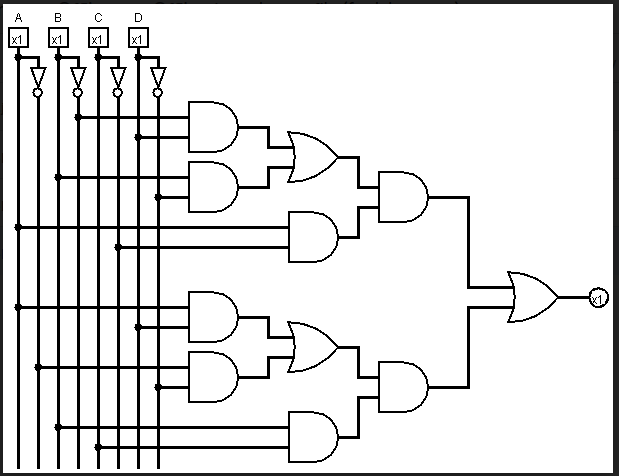
**Required Equation:**

F (A, B, C, D) = A’BCD’ + AB’C’D + ABC’D’ + ABCD

= BC (AD + A’D’) + AC’ (B’D + BD’)

= BC (A ⊕ D)’ + AC’ (B ⊕ D)

**Circuit Diagram:**



**Observations:**

1. We tried to make the circuit in such a way that it was not too dense with wires
2. We used the documentations of the ICs to make sure the connections were given through the right pins
3. We checked the output according to the truth table